CMS80F731x Datasheet

Enhanced flash 8-bit 1T 8051 microcontroller

Rev.1.0.2

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1. Product Features

1.1 Features

- **Compatible with mcS-51's 1T command system**
  - The system clock frequency supports up to 48 MHz
  - The machine cycle is supported up to 1T_{SYS} @ F_{SYS}≤24MHz
  - The fastest machine cycle supports 2T_{SYS} @ F_{SYS}= 48MHz
- **memory**
  - Program FLASH: 16K×8Bit
  - Data FLASH：1K×8Bit
  - General RAM: 256×8Bit
  - Universal XRAM: 1K×8Bit
  - Support BOOT region, 1K/2K/4K optional
  - The program FLASH supports partition protection
- **4 oscillation modes**
  - HSI - Internal high-speed oscillation: 48MHz
  - HSE-External high-speed oscillation: 8MHz/16MHz
  - LSE-External low-speed oscillation: 32.768KHz
  - LSI - Internal low-speed oscillation: 125KHz
- **GPIO**
  - Up to 26 GPIOs
  - Both support pull-up/down resistor function
  - Both support edge (rising/falling/double-edge) interrupts
  - Both support wake-up function
- **Interrupt source**
  - All external port interrupts are supported
  - 7 timer interrupts
  - Other peripheral interrupts
- **timer**
  - WDT Timer (Watchdog Timer)
  - Timer0/1，Timer2，Timer3/4
  - LSE_Timer (supports sleep wake-up function).
  - WUT (wake-up timer)
  - BRT (Serial Port Baud Rate Clock Generator)
- **Cyclic redundancy check cell**
  - CRC16（CRC16-CCITT）
- **Buzzer driver**
  - 50% duty cycle, frequency can be set freely
- **PWM**
  - 6-channel PWM
  - 6 mutually independent cycle counters
  - Supports independent/complementary/synchronous/grouped modes
  - Edge alignment is supported
  - Supports complementary mode dead-zone delay function
- **Operating voltage range**
  - 2.1V~5.5V
- **Operating temperature range**
  - -40℃~105℃
- **Low Voltage Reset Function (LVR)**
  - 1.8V/2.0V/2.5V/3.5V
- **Low Voltage Detection Function (LVD)**
  - 2.0V~4.3V 8 levels selectable
- **High Precision 12-bit ADC**
  - Up to 26 AD external channels
  - Reference Voltage Selectable (1.2V/2.0V/2.4V/3.0V/VDD)
  - detectable Internal 1.2V reference voltage
  - Supports hardware-triggered start conversion features
  - Supports a set of result number comparison functions
- **High sensitivity touch**
- **Hardware LED matrix driver**
  - Duty cycle 1/4, 1/5, 1/6, 1/8 selectable
  - Supports two modes of common-negative/common-positive
  - Three clock sources are available, LSI/LSE/system clock
  - COM, SEG current selectable
  - Supports up to 4COM x 16SEG, 5COM x 15SEG 6COM x 14SEG, 8COM x 12SEG
- **Hardware LED dot matrix driver**
  - Three clock sources are available, LSI/LSE/system clock
  - Supports both cyclic and interrupt scans
  - Supports each lamp display data optionally
  - Supports two on-time options per lamp
  - Current 16 gears are available
  - Supports up to 9 pin drives and up to 64 lamp drivers Choose from dot matrix 4x4, 5x5, 6x6, 6x7, 7x7, 7x8, 8x8
- **Low-power mode**
  - Idle mode (IDLE)
  - Sleep Mode (STOP)
- **Supports 96-bit unique ID number (UID)**
  - Each chip has a separate ID number
- **Supports two-wire serial programming and debugging**
- **Communication module**
  - 1xSPI (communication rate up to 6Mb/s)
  - 1xI2C (communication rate up to 400Kb/s)
  - 2xUART (baud rate up to 1Mb/s). UART1 can be mapped arbitrarily by GPIO

1.2 Product Comparison

Peripheral interface \ Product		CMS80F7316	CMS80F7318
Maximum clock frequency		48MHz	
Storage Module	APROM	16/15/14/12 KB(1)	
	BOOT	0/1/2/4 KB(1)	
	Data FLASH	1 KB	
	RAM	256 B	
	XRAM	1 KB	
timer	WDT	1	
	Timer0/1	2 (16bit)	
	Timer2	1 (16bit)	
	Timer3/4	2 (16bit)	
	LSE_Timer	1 (16bit)	
	WUT	1 (12bit)	
	BRT	1 (16bit)	
Enhanced Digital peripherals	CRC	CRC16-CCITT	
	BUZZER	1	
	PWM	6(16bit)	
Displays the interface	LED matrix	4COM x 9SEG, 5COM x 8SEG 6COM x 7SEG, 8COM x 5SEG	4COM x 16SEG, 5COM x 15SEG 6COM x 14SEG, 8COM x 12SEG
	LED dot matrix	4x4, 5x5, 6x6, 6x7, 7x7, 7x8, 8x8	
Communication module	SPI	1	
	I2C	1	
	UART	2	
Analog module	12bit-ADC (Number of external channels)	18	26
	TOUCH	18	26
GPIOs		18	26
LVR		1.8V/2.0V/2.5V/3.5V	
LVD		2.0~4.3 V,8 levels	
Operating voltage		2.1~5.5 V	
Operating temperature		-40~105℃	
packaging		SOP20、TSSOP20	SOP28、SSOP28

Note: (1) The SIZE OF THE APROM and BOOT SPACE IS SET THROUGH THE SYSTEM CONFIGURATION REGISTER, AND THE TOTAL MAXIMUM APROM AND BOOT SPACE IS 16K.

2. System Overview

2.1 System Introduction

The series is an 8051 core, MCS-51 compatible 1T command system, a general-purpose IO type 8-bit chip, operating frequency up to 48MHz, the MCU has the following features:

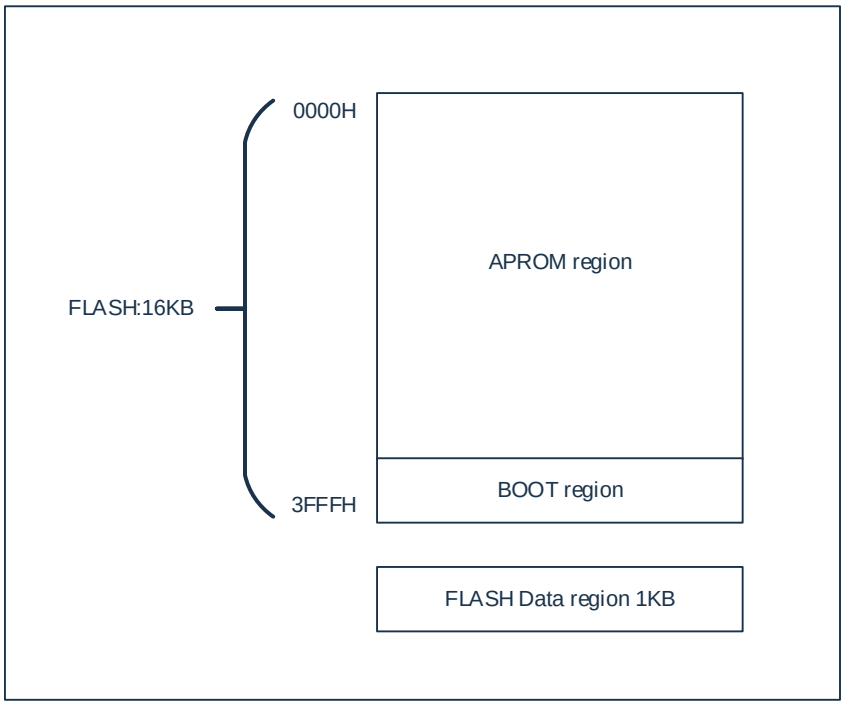
- Features a maximum of 16KB of program area, 256B of RAM space, 1KB of XRAM, and 1KB of non-volatile data area.
- With four oscillation modes, the system clock can be freely switched between three clock sources (HSE and LSE are prohibited from switching to each other), and external oscillator stop detection.
- Support normal, idle, sleep three working modes, can effectively reduce power consumption.
- Built-in low-voltage reset LVR, low-voltage monitoring LVD, watchdog overflow reset and other protection settings can effectively improve the reliability of system operation.
- It has a variety of interrupt sources such as external interrupts, timer interrupts and other peripheral interrupts, which can respond to external events in a timely manner and improve the utilization of MCUs.
- Up to 9 timers, can achieve timing, counting, input capture, output comparison, timed wake-up, baud rate generator and other functions.
- Has a cyclic redundancy check unit CRC.
- Up to 8COM and 16SEG LED matrix drive, 8x 8 LED dot matrix drive.
- Six 16-bit PWMs support independent, complementary, synchronous three modes of output, while with dead-zone control function.
- With 1 I2C, 1 SPI, 2 UART communication modules, it can realize data transmission between the system and other devices.
- Features a high accuracy 12-bit ADC with selectable internal reference voltage.
- Touch with high sensitivity.

2.2 Memory Structure

2.2.1 Program Memory FLASH

The chip has a 16KB flash storage space, and the APROM area and the BOOT area share the entire FLASH space.

The flash space allocation block diagram is as follows:

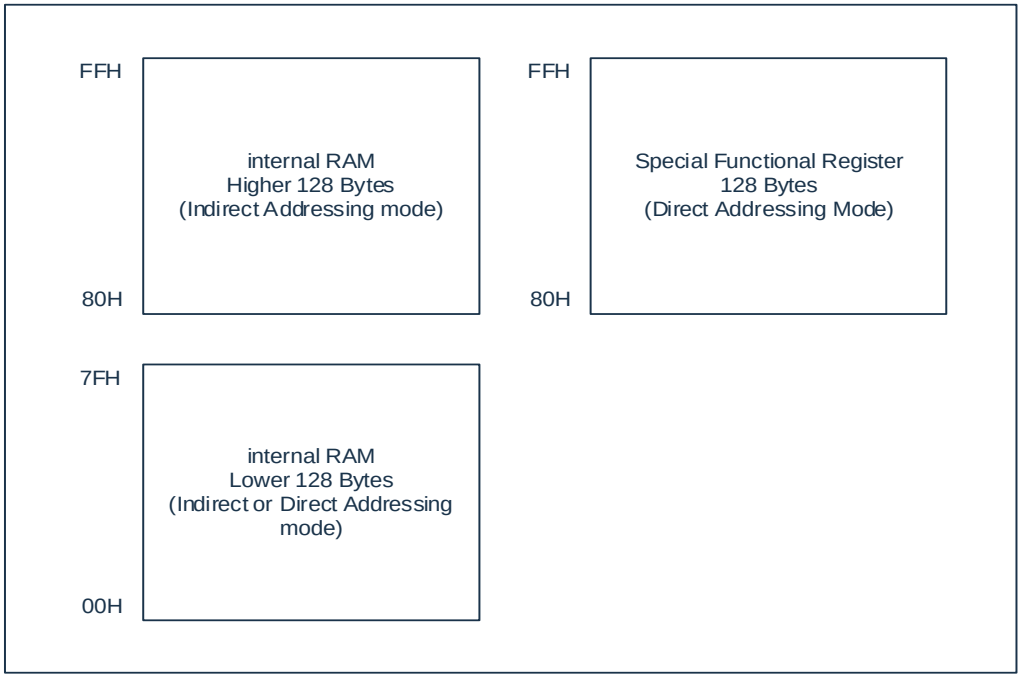


The size of the BOOT can be configured as follows:

16K (Program storage area)				
Address space allocation	APROM area		BOOT area	
Mode 0	16K	0000H-3FFFH	--	--
Mode 1	15K	0000H-3BFFH	1K	3C00H-3FFFH
Mode 2	14K	0000H-37FFH	2K	3800H-3FFFH
Mode 3	12K	0000H-2FFFH	4K	3000H-3FFFH

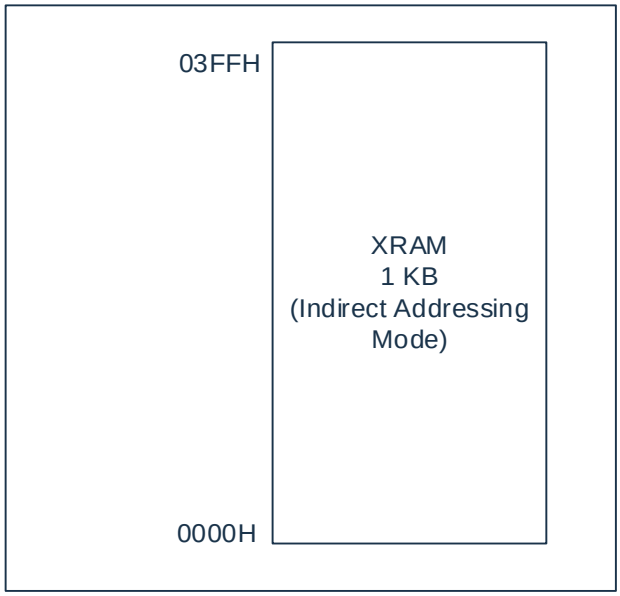
2.2.2 Internal Data Memory RAM

The internal data memory is divided into 3 parts: low 128Bytes, high 128Bytes, SFR. The RAM space allocation block diagram is shown in the following figure:



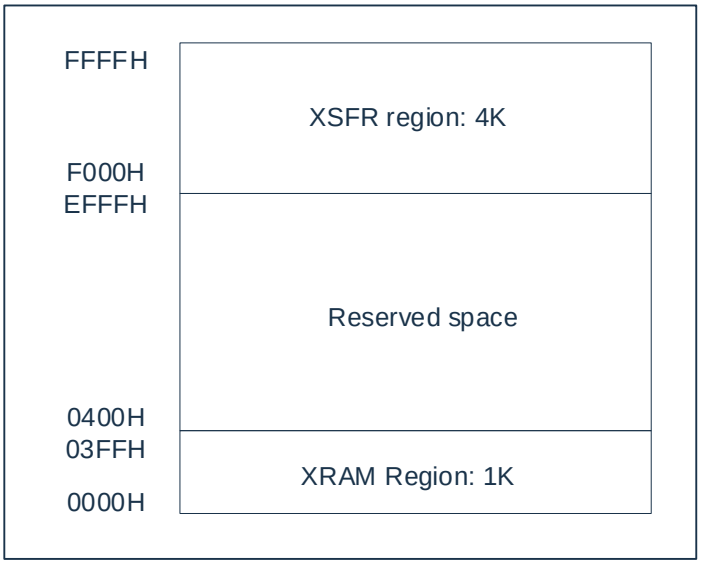
2.2.3 External Data Memory XRAM

There is a 1KB XRAM area inside the chip, which is not connected to RAM/FLASH, and the XRAM space allocation block diagram is shown in the following figure.



2.2.4 Special Function Register XSFR

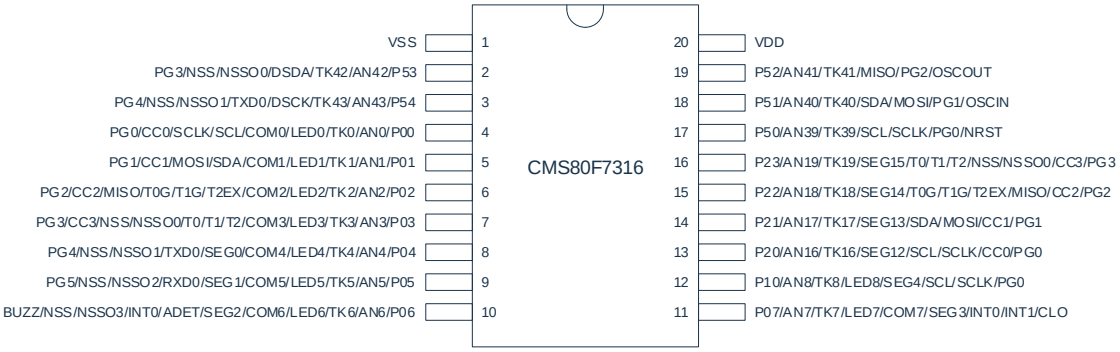
XSFR is a special register shared by the addressing space and XRAM, mainly including: port control registers, other function control registers. Its addressing range is as follows:



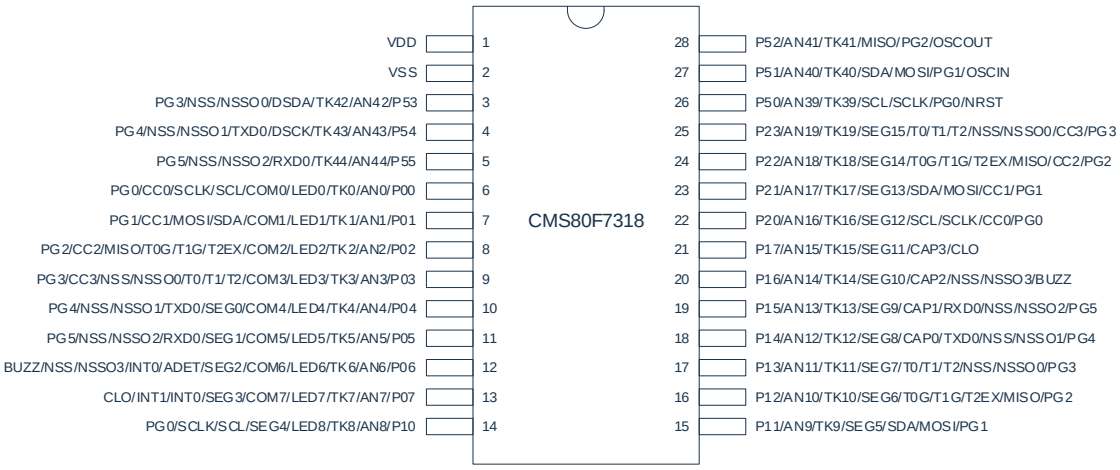
3. Pin Definition

3.1 Pin Description

3.1.1 CMS80F7316-pin Figure (SOP20/TSSOP20)



3.1.2 CMS80F7318-pin Figure (SOP28/SSOP28)



3.2 Pin Function Description

Symbol description: I/O represents digital input/output, I represents digital input, O represents digital output, AI represents analog input, and AO represents analog output.

Pin number		Pin name	Pin type	description
CMS80F7316	CMS80F7318			
SOP20/TSSOP20	SOP28/SSOP28			
4	6	P00	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
		AN0	AI	ADC channel 0 input
		TK0	AI	Touch key channel 0 input
		COM0	O	LED COM0 output
		LED0	O	LED dot matrix scan LED0 output
		SCL	I/O	I2C clock input and output
		SCLK	I/O	SPI clock input and output
		CC0	O	Timer2 compare output channel 0
		PG0	O	PWM channel 0 output
		TXD1	O	UART1 data output
		RXD1	I/O	UART1 data input/synchronous mode data output
5	7	P01	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
		AN1	AI	ADC channel 1 input
		TK1	AI	Touch key channel 1 input
		COM1	O	LED COM1 output
		LED1	O	LED dot matrix scan LED1 output
		SDA	I/O	I2C data input and output
		MOSI	I/O	SPI data master sends slave receive
		CC1	O	Timer2 compare output channel 1
		PG1	O	PWM channel 1 output
		TXD1	O	UART1 data output
		RXD1	I/O	UART1 data input/synchronous mode data output
6	8	P02	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
		AN2	AI	ADC channel 2 input
		TK2	AI	Touch key channel 2 input
		COM2	O	LED COM2 output
		LED2	O	LED dot matrix scan LED2 output

Pin number		Pin name	Pin type	description
CMS80F7316	CMS80F7318			
SOP20/TSSOP20	SOP28/SSOP28			
		T0G	I	Timer0 gated input
		T1G	I	Timer1 gated input
		T2EX	I	Timer2 drops along the auto-reload input
		MISO	I/O	The SPI data master receives the slave send
		CC2	O	Timer2 compare output channel 2
		PG2	O	PWM channel 2 output
		TXD1	O	UART1 data output
		RXD1	I/O	UART1 data input/synchronous mode data output
7	9	P03	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
		AN3	AI	ADC channel 3 input
		TK3	AI	Touch key channel 3 input
		COM3	O	LED COM3 output
		LED3	O	LED dot matrix scan LED3 output
		T0	I	Timer0 external clock input
		T1	I	Timer1 external clock input
		T2	I	Timer2 external event or gated input
		NSS(NSSO0)	I/O	The SPI selects input from the control/main control select 0 output
		CC3	O	Timer2 compare output channel 3
		PG3	O	PWM channel 3 output
		TXD1	O	UART1 data output
		RXD1	I/O	UART1 data input/synchronous mode data output
8	10	P04	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
		AN4	AI	ADC channel 4 input
		TK4	AI	Touch key channel 4 input
		SEG0	O	LED SEG0 output
		COM4	O	LED COM4 output
		LED4	O	LED dot matrix scan LED4 output
		TXD0	O	UART0 data output
		NSS(NSSO1)	I/O	The SPI is selected from the control select input/master select 1 output
		PG4	O	PWM channel 4 output

Pin number		Pin name	Pin type	description
CMS80F7316	CMS80F7318			
SOP20/TSSOP20	SOP28/SSOP28			
		TXD1	O	UART1 data output
		RXD1	I/O	UART1 data input/synchronous mode data output
9	11	P05	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
		AN5	AI	ADC channel 5 input
		TK5	AI	Touch key channel 5 input
		SEG1	O	LED SEG1 output
		COM5	O	LED COM5 output
		LED5	O	LED dot matrix scan LED5 output
		RXD0	I/O	UART0 data input/synchronous mode data output
		NSS(NSSO2)	I/O	The SPI selects input from the control/main control select 2 output
		PG5	O	PWM channel 5 output
		TXD1	O	UART1 data output
		RXD1	I/O	UART1 data input/synchronous mode data output
10	12	P06	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
		AN6	AI	ADC channel 6 input
		TK6	AI	Touch key channel 6 input
		SEG2	O	LED SEG2 output
		COM6	O	LED COM6 output
		LED6	O	LED dot matrix scan LED6 output
		CUSTOM	I	ADC external trigger input
		INT0	I	External interrupt 0 input
		NSS(NSSO3)	I/O	The SPI selects input from the control/main control select 3 output
		BUZZ	O	Buzzer drive output
		TXD1	O	UART1 data output
		RXD1	I/O	UART1 data input/synchronous mode data output
11	13	P07	I/O	GPIO configure input and output through registers, pull up, pull down and other functions

Pin number		Pin name	Pin type	description
CMS80F7316	CMS80F7318			
SOP20/TSSOP20	SOP28/SSOP28			
		AN7	AI	ADC channel 7 input
		TK7	AI	Touch key channel 7 input
		SEG3	O	LED SEG3 output
		COM7	O	LED COM7 output
		LED7	O	LED dot matrix scan LED7 output
		INT0	I	External interrupt 0 input
		INT1	I	External interrupt 1 input
		CLO	O	System clock divider output
		TXD1	O	UART1 data output
		RXD1	I/O	UART1 data input/synchronous mode data output
12	14	P10	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
		AN8	AI	ADC channel 8 input
		TK8	AI	Touch key channel 8 input
		SEG4	O	LED SEG4 output
		LED8	O	LED dot matrix scan LED8 output
		SCL	I/O	I2C clock input and output
		SCLK	I/O	SPI clock input and output
		PG0	O	PWM channel 0 output
		TXD1	O	UART1 data output
		RXD1	I/O	UART1 data input/synchronous mode data output
-	15	P11	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
		AN9	AI	ADC channel 9 input
		TK9	AI	Touch key channel 9 input
		SEG5	O	LED SEG5 output
		SDA	I/O	I2C data input and output
		MOSI	I/O	SPI data master sends slave receive
		PG1	O	PWM channel 1 output
		TXD1	O	UART1 data output
		RXD1	I/O	UART1 data input/synchronous mode data output
-	16	P12	I/O	GPIO configure input and output through registers, pull up, pull down and other

Pin number		Pin name	Pin type	description
CMS80F7316	CMS80F7318			
SOP20/TSSOP20	SOP28/SSOP28			
				functions
		AN10	AI	ADC channel 10 input
		TK10	AI	Touch key channel 10 input
		SEG6	O	LED SEG6 output
		T0G	I	Timer0 gated input
		T1G	I	Timer1 gated input
		T2EX	I	Timer2 drops along the auto-reload input
		MISO	I/O	The SPI data master receives the slave send
		PG2	O	PWM channel 2 output
		TXD1	O	UART1 data output
		RXD1	I/O	UART1 data input/synchronous mode data output
-	17	P13	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
		AN11	AI	ADC channel 11 input
		TK11	AI	Touch key channel 11 input
		SEG7	O	LED SEG7 output
		T0	I	Timer0 external clock input
		T1	I	Timer1 external clock input
		T2	I	Timer2 external event or gated input
		NSS(NSSO0)	I/O	The SPI selects input from the control/main control select 0 output
		PG3	O	PWM channel 3 output
		TXD1	O	UART1 data output
		RXD1	I/O	UART1 data input/synchronous mode data output
-	18	P14	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
		AN12	AI	ADC channel 12 input
		TK12	AI	Touch key channel 12 input
		SEG8	O	LED SEG8 output
		CAP0	I	Timer2 input capture channel 0
		TXD0	O	UART0 data output
		NSS(NSSO1)	I/O	The SPI is selected from the control select input/master select 1 output
		PG4	O	PWM channel 4 output

Pin number		Pin name	Pin type	description
CMS80F7316	CMS80F7318			
SOP20/TSSOP20	SOP28/SSOP28			
		TXD1	O	UART1 data output
		RXD1	I/O	UART1 data input/synchronous mode data output
-	19	P15	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
		AN13	AI	ADC channel 13 input
		TK13	AI	Touch key channel 13 input
		SEG9	O	LED SEG9 output
		CAP1	I	Timer2 input capture channel 1
		RXD0	I/O	UART0 data input/synchronous mode data output
		NSS(NSSO2)	I/O	The SPI selects input from the control/main control select 2 output
		PG5	O	PWM channel 5 output
		TXD1	O	UART1 data output
		RXD1	I/O	UART1 data input/synchronous mode data output
-	20	P16	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
		AN14	AI	ADC channel 14 input
		TK14	AI	Touch key channel 14 input
		SEG10	O	LED SEG10 output
		CAP2	I	Timer2 input capture channel 2
		NSS(NSSO3)	I/O	The SPI selects input from the control/main control select 3 output
		BUZZ	O	Buzzer drive output
		TXD1	O	UART1 data output
		RXD1	I/O	UART1 data input/synchronous mode data output
-	21	P17	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
		AN15	AI	ADC channel 15 input
		TK15	AI	Touch key channel 15 input
		SEG11	O	LED SEG11 output
		CAP3	I	Timer2 input capture channel 3

Pin number		Pin name	Pin type	description
CMS80F7316	CMS80F7318			
SOP20/TSSOP20	SOP28/SSOP28			
		CLO	O	System clock divider output
		TXD1	O	UART1 data output
		RXD1	I/O	UART1 data input/synchronous mode data output
13	22	P20	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
		AN16	AI	ADC channel 16 input
		TK16	AI	Touch key channel 16 input
		SEG12	O	LED SEG12 output
		SCL	I/O	I2C clock input and output
		SCLK	I/O	SPI clock input and output
		CC0	O	Timer2 compare output channel 0
		PG0	O	PWM channel 0 output
		TXD1	O	UART1 data output
		RXD1	I/O	UART1 data input/synchronous mode data output
14	23	P21	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
		AN17	AI	ADC channel 17 input
		TK17	AI	Touch key channel 17 input
		SEG13	O	LED SEG13 output
		SDA	I/O	I2C data input and output
		MOSI	I/O	SPI data master sends slave receive
		CC1	O	Timer2 compare output channel 1
		PG1	O	PWM channel 1 output
		TXD1	O	UART1 data output
		RXD1	I/O	UART1 data input/synchronous mode data output
15	24	P22	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
		AN18	AI	ADC channel 18 input
		TK18	AI	Touch key channel 18 input
		SEG14	O	LED SEG14 output
		T0G	I	Timer0 gated input
		T1G	I	Timer1 gated input

Pin number		Pin name	Pin type	description
CMS80F7316	CMS80F7318			
SOP20/TSSOP20	SOP28/SSOP28			
		T2EX	I	Timer2 drops along the auto-reload input
		MISO	I/O	The SPI data master receives the slave send
		CC2	O	Timer2 compare output channel 2
		PG2	O	PWM channel 2 output
		TXD1	O	UART1 data output
		RXD1	I/O	UART1 data input/synchronous mode data output
16	25	P23	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
		AN19	AI	ADC channel 19 input
		TK19	AI	Touch key channel 19 input
		SEG15	O	LED SEG15 output
		T0	I	Timer0 external clock input
		T1	I	Timer1 external clock input
		T2	I	Timer2 external event or gated input
		NSS(NSSO0)	I/O	The SPI selects input from the control/main control select 0 output
		CC3	O	Timer2 compare output channel 3
		PG3	O	PWM channel 3 output
		TXD1	O	UART1 data output
		RXD1	I/O	UART1 data input/synchronous mode data output
17	26	P50	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
		AN39	AI	ADC channel 39 input
		TK39	AI	Touch key channel 39 input
		NRST	I	External reset input
		SCL	I/O	I2C clock input and output
		SCLK	I/O	SPI clock input and output
		PG0	O	PWM channel 0 output
		TXD1	O	UART1 data output
		RXD1	I/O	UART1 data input/synchronous mode data output
18	27	P51	I/O	GPIO configure input and output through registers, pull up, pull down and other functions

Pin number		Pin name	Pin type	description
CMS80F7316	CMS80F7318			
SOP20/TSSOP20	SOP28/SSOP28			
		AN40	AI	ADC channel 40 input
		TK40	AI	Touch key channel 40 input
		OSCIN	AI	External oscillation HSE/LSE input
		SDA	I/O	I2C data input and output
		MOSI	I/O	SPI data master sends slave receive
		PG1	O	PWM channel 1 output
		TXD1	O	UART1 data output
		RXD1	I/O	UART1 data input/synchronous mode data output
19	28	P52	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
		AN41	AI	ADC channel 41 input
		TK41	AI	Touch key channel 41 input
		OSCOUT	AO	External oscillation HSE/LSE output
		MISO	I/O	The SPI data master receives the slave send
		PG2	O	PWM channel 2 output
		TXD1	O	UART1 data output
		RXD1	I/O	UART1 data input/synchronous mode data output
2	3	P53	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
		AN42	AI	ADC channel 42 input
		TK42	AI	Touch key channel 42 input
		DSDA	I/O	Programming/debugging data input and output ports
		NSS(NSSO0)	I/O	The SPI selects input from the control/main control select 0 output
		PG3	O	PWM channel 3 output
		TXD1	O	UART1 data output
		RXD1	I/O	UART1 data input/synchronous mode data output
3	4	P54	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
		AN43	AI	ADC channel 43 input
		TK43	AI	Touch key channel 43 input

Pin number		Pin name	Pin type	description
CMS80F7316	CMS80F7318			
SOP20/TSSOP20	SOP28/SSOP28			
		DSCK	I/O	Programming/debugging clock inputs/outputs
		TXD0	O	UART0 data output
		NSS(NSSO1)	I/O	The SPI is selected from the control select input/master select 1 output
		PG4	O	PWM channel 4 output
		TXD1	O	UART1 data output
		RXD1	I/O	UART1 data input/synchronous mode data output
-	5	P55	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
		AN44	AI	ADC channel 44 input
		TK44	AI	Touch key channel 44 input
		RXD0	I/O	UART0 data input/synchronous mode data output
		NSS(NSSO2)	I/O	The SPI selects input from the control/main control select 2 output
		PG5	O	PWM channel 5 output
		TXD1	O	UART1 data output
		RXD1	I/O	UART1 data input/synchronous mode data output
20	1	InDD	P	Supply voltage input pin
1	2	VSS	P	Grounding feet

3.3 GPIO Features

Pins are shared in a variety of functions, and each I/O port can be flexibly configured with digital functions or specified analog functions. I/O as a universal GPIO port has the following characteristics:

- 2 levels I/O output slope can be configured.
- Data latch status or pin status can be read.
- Configurable rising, falling, and dual edge trigger interrupts.
- Configurable rising, falling, and dual-edge interrupt wake-up chip.
- It can be configured as normal input, pull-up input, pull-down input, push-pull output, open-drain output mode.

3.4 List of Pin Functions

List of digital function ports:

	External input	Digital function configuration							
		0	1	2	3	4	5	6	7
P00	-	GPIO	ANA	SCL	SCLK	CC0	PG0	TXD1	RXD1
P01	-	GPIO	ANA	SDA	MOSI	CC1	PG1	TXD1	RXD1
P02	T0G/T1G/T2EX	GPIO	ANA	-	MISO	CC2	PG2	TXD1	RXD1
P03	T0/T1/T2	GPIO	ANA	-	NSS(NSSO0)	CC3	PG3	TXD1	RXD1
P04	-	GPIO	ANA	TXD0	NSS(NSSO1)	-	PG4	TXD1	RXD1
P05	-	GPIO	ANA	RXD0	NSS(NSSO2)	-	PG5	TXD1	RXD1
P06	MOQ/INT0	GPIO	ANA	-	NSS(NSSO3)	BUZZ	-	TXD1	RXD1
P07	INT0/INT1	GPIO	ANA	-	-	CLO	-	TXD1	RXD1
P10	-	GPIO	ANA	SCL	SCLK	-	PG0	TXD1	RXD1
P11	-	GPIO	ANA	SDA	MOSI	-	PG1	TXD1	RXD1
P12	T0G/T1G/T2EX	GPIO	ANA	-	MISO	-	PG2	TXD1	RXD1
P13	T0/T1/T2	GPIO	ANA	-	NSS(NSSO0)	-	PG3	TXD1	RXD1
P14	CAP0	GPIO	ANA	TXD0	NSS(NSSO1)	-	PG4	TXD1	RXD1
P15	CAP1	GPIO	ANA	RXD0	NSS(NSSO2)	-	PG5	TXD1	RXD1
P16	CAP2	GPIO	ANA	-	NSS(NSSO3)	BUZZ	-	TXD1	RXD1
P17	CAP3	GPIO	ANA	-	-	CLO	-	TXD1	RXD1
P20	-	GPIO	ANA	SCL	SCLK	CC0	PG0	TXD1	RXD1
P21	-	GPIO	ANA	SDA	MOSI	CC1	PG1	TXD1	RXD1
P22	T0G/T1G/T2EX	GPIO	ANA	-	MISO	CC2	PG2	TXD1	RXD1
P23	T0/T1/T2	GPIO	ANA	-	NSS(NSSO0)	CC3	PG3	TXD1	RXD1
P50	NSRT	GPIO	ANA	SCL	SCLK	-	PG0	TXD1	RXD1
P51	-	GPIO	ANA	SDA	MOSI	-	PG1	TXD1	RXD1
P52	-	GPIO	ANA	-	MISO	-	PG2	TXD1	RXD1
P53	-	GPIO	ANA	-	NSS(NSSO0)	-	PG3	TXD1	RXD1
P54	-	GPIO	ANA	TXD0	NSS(NSSO1)	-	PG4	TXD1	RXD1
P55	-	GPIO	ANA	RXD0	NSS(NSSO2)	-	PG5	TXD1	RXD1

List of LED ports, analog ports, CONFIG configuration ports:

	GPIO(0)			ANA(1)						CONFIG
	LEDSEG	LEDCOM	LEDx	ADC	TOUCH					
P00	-	COM0	LED0	AN0	TK0					-
P01	-	COM1	LED1	AN1	TK1					-
P02	-	COM2	LED2	AN2	TK2					-
P03	-	COM3	LED3	AN3	TK3					-
P04	SEG0	COM4	LED4	AN4	TK4					-
P05	SEG1	COM5	LED5	AN5	TK5					-
P06	SEG2	COM6	LED6	AN6	TK6					-
P07	SEG3	COM7	LED7	AN7	TK7					-
P10	SEG4	-	LED8	AN8	TK8					-
P11	SEG5	-		AN9	TK9					-
P12	SEG6	-		AN10	TK10					-
P13	SEG7	-		AN11	TK11					-
P14	SEG8	-		AN12	TK12					-
P15	SEG9	-		AN13	TK13					-
P16	SEG10	-		AN14	TK14					-
P17	SEG11	-		AN15	TK15					-
P20	SEG12	-		AN16	TK16					-
P21	SEG13	-		AN17	TK17					-
P22	SEG14	-		AN18	TK18					-
P23	SEG15	-		AN19	TK19					-
P50	-	-		AN39	TK39					NRST
P51	-	-		AN40	TK40					OSCIN
P52	-	-		AN41	TK41					OSCOUT
P53	-	-		AN42	TK42					DSDA
P54	-	-		AN43	TK43					DSCK
P55	-	-		AN44	TK44					-

Note: The chip pins are subject to the actual chip.

4. Feature Summary

4.1 System Clock

The system clock has four clock sources, which can be selected by setting the system configuration register or user register. The system clock module has the following features:

- Selectable internal high-speed oscillation HSI (48MHz).
- Optional external high-speed crystal oscillation HSE (8MHz/16MHz).
- Optional external low-speed crystal oscillation LSE (32.768KHz).
- Optional internal low-speed oscillation LSI (125KHz).
- Any two clock sources can be switched to each other (switching is prohibited between HSE and LSE).
- External high-speed and low-speed oscillators provide a stop-oscillation monitoring function (SCM) when the system clock is provided.

4.2 Reset

The reset operation is used to initialize the internal circuitry of the chip, allowing the system to start working from a determined state. The chip has the following reset methods:

- Power-on reset.
- External reset.
- Low voltage reset.
- CONFIG status protection reset.
- Power-on configuration monitor reset.
- Watchdog overflow reset.
- Software reset.

Any of the above reset situations require a certain response time, and the system provides a perfect reset process to ensure the smooth progress of the reset operation.

4.3 Power Management

4.3.1 Working Mode

The chip has 3 different operating modes to adapt to the power consumption requirements of different applications.

- Normal operating mode: The MCU is in normal working condition and the peripherals are operating normally.
- Idle mode IDLE: The MCU is in idle mode, the CPU stops working, and the peripherals are running normally. This mode can be woken up by any interrupt.
- Hibernate mode STOP: The MCU is in sleep mode, the CPU stops working, and the peripherals stop working. This mode can be woken up by INT0/1 interrupt, GPIO interrupt wake-up, WUT timed wake-up, LSE timed wake-up.

4.3.2 Power Supply Low Voltage Reset (LVR)

When the supply voltage falls below the set sense voltage, the system resets.

There are four options for low-voltage reset: 1.8V/2.0V/2.5V/3.5V.

4.3.3 Power Supply Low Voltage Detection (LVD)

The low voltage detection circuit compares the supply voltage to the set voltage and generates an interrupt request signal if the supply voltage is lower than the set voltage.

The programmable detection voltage range is 2.0V to 4.3V, and a total of 8 levels are available.

4.4 Interrupt Control

The chip has multiple interrupt sources and interrupt vectors, user-programmable interrupts include INT0/1, Timer0/1, Timer2, Timer3/4, WDT, LSE_Timer (SCM), PWM, I2C, SPI, UART0/1, P0/P1/P2/P5, ADC, LVD, LED, TOUCH The actual number of interrupt sources varies by product.

The chip specifies two interrupt priorities, allowing for two levels of interrupt nesting. When an interrupt has already responded, if a high-level interrupt is requested, the latter can interrupt the former, realizing interrupt nesting.

4.5 Timer

4.5.1 WDT Timer

The watchdog timer is an on-chip timer that is provided by the system clock and overflows with WDT timing will produce a reset. Watchdog reset is a protective setting of the system, when the system is running to an unknown state, the watchdog can be used to reset the system, thereby avoiding the system from entering an indefinite dead loop. WDT timers have the following features:

- Watchdog overflow time 8 levels optional.
- Watchdog overflow interrupt can be set.
- Watchdog overflow reset can be set.

4.5.2 Timer Counter 0/1 (Timer0/1)

Timer 0 is similar in type and structure to Timer 1 and is two 16-bit up counting timers. Timer0 has 4 modes of operation and Timer1 has 3 modes of operation, which provide basic timing and event counting operations.

In "timer mode", the timing register is incremented every 12 or 4 system cycles when the timer clock is enabled. In "counter mode", the timing register increments whenever it detects a falling edge on the corresponding input pin (T0 or T1). Timer0/1 has the following features:

- Can be used as a normal timer.
- Can be used for gated timer functions.
- External counting function can be implemented.
- Can be used for gated counting functions.
- The counter overflow interrupts.

4.5.3 Timer Counter 2 (Timer2)

Timer 2 is a 16-bit timer that can be used for the generation of various digital signals and event capture, such as pulse generation, pulse width modulation, pulse width measurement, etc. Timer2 has the following features:

- Can be used as a normal timer.
- Can be used for gated Timer functions.
- External counting function can be implemented.
- It has the functions of reload prohibition, overflow automatic reload, and automatic reloading of external pin falling edge.
- Capture can be triggered by the rising edge, falling edge, double edge, or low byte of the write capture register.
- Features a comparison function that generates a periodic signal with a controllable duty cycle of the PWM waveform.
- Timing, external triggering, capture, and comparison can all produce interrupts.

4.5.4 Timer 3/4 (Timer3/4)

Timer 3/4 is similar to timer 0/1 in that it is two 16-bit timers. Timer3 has 4 working modes and Timer4 has 3 working modes. In contrast to Timer0/1, Timer3/4 only provides timer operations.

With the timer activated, the value of the register is incremented every 12 or 4 system cycles.

4.5.5 LSE Timer(LSE_Timer)

The LSE timer is a clock source from an external low-speed clock LSE, a 16-bit up-counting timer. LSE timers have the following features:

- Timer function.
- A 16-bit timer value can be set.
- Works in sleep mode.
- An interrupt can occur when the count value is equal to the timer value.
- A timed interrupt wakes up idle mode/sleep mode.

4.5.6 Wake-up Timer (WUT)

The WUT wake-up timer is a clock source from the internal low-speed clock LSI, a 12-bit, up-count timer for sleep wake-ups. After the system enters sleep mode, the CPU stops working with all peripheral circuitry, and the internal low-speed clock LSI provides a clock to the WUT counter. WUT has the following features:

- The system can be woken up at a configured time during sleep.
- The counting clock is available in divide-by-1, 8, 32, and 256.
- A 12-bit timer value can be set.

4.5.7 Baud Rate Generator (BRT)

The BRT timer is a 16-bit baud rate timer whose clock source comes from the system clock and primarily provides a clock for the UART module. BRTs have the following features:

- Has an independent control switch.
- The counting clock has an 8-levels frequency division option.
- 16-bit increment count.

4.6 Enhanced digital peripherals

4.6.1 Cyclic Redundancy Check Unit (CRC)

Cyclic redundancy check CRC is the most commonly used error check code in the field of data communication, which is characterized by the length of the information field and the check field can be arbitrarily selected. The chip CRC check unit generates polynomials using "$X^{16}+X^{12}+X^5+1$" (CRC16-CCITT) to program the data to be verified, so that the module is not limited to the code flash memory area and can be used for multi-purpose checks.

4.6.2 Buzzer Driver (BUZZER)

The buzzer drive module consists of an 8-bit counter, clock driver, control register, and a square wave with an output duty cycle of 50% and a frequency covering a wide range. BUZZER has the following features:

- Has a separate enable control switch.
- The clock division ratio of 8, 16, 32, and 64 can be set.
- The output frequency is 8-bit controllable, and the output can be set (1~255) x 2 frequency division.

4.6.3 PWM module

The PWM module supports 6-channel PWM generators with independently programmable cycles and duty cycles. PWM has the following features:

- Supports two kinds of waveform outputs in single-shot and continuous mode.
- Supports four control modes: independent, complementary, synchronous, and group control.
- The counting clocks are available in divide-by-1, 2, 4, 8, and 16.
- Edge alignment mode is supported.
- Supports dead-zone programming.
- Output polarity can be set.
- Supports downward comparison and zero point interrupt.

4.7 Display Interface

4.7.1 Hardware LED Matrix Driver Module

The hardware LED matrix driver module can easily realize the display driver of the LED. The module has the following features:

- 1/4, 1/5, 1/6, 1/8 4 types of DUTY can be selected.
- Three clock sources are available: system clock, LSI, and LSE.
- 16-bit clock source frequency division controller.
- COM port common-negative, common-positive two drive mode optional.
- Supports up to 8 COM ports and 16SEG ports.
- Each COM and SEG port has an enable control bit.
- COM port current 50mA, 150mA two levels are selectable (V_{OL}= 1.5V@VDD = 5V).
- The SEG port current is selectable in 16 levels, and the maximum current can reach 40mA (V_{OH}=3.5V@VDD=5V).

4.7.2 Hardware LED Dot Matrix Driver Module

The hardware LED dot matrix driver module can easily realize the LED dot matrix driver. The module has the following features:

- Up to 9 LED0-LED8 pin enables are available.
- Supports up to 64 led drivers, with dot matrix 4x4, 5x5, 6x6, 6x7, 7x7, 7x8, 8x8.
- Each lamp supports two on-time options, each with a 16-bit timing setting.
- Each lamp display data is selectable.
- System clock source, LSI, LSE three selection.
- 16-bit clock source frequency division controller.
- Both cyclic scan mode and interrupt scan mode are supported.
- Current 16 levels are available and the maximum current can reach 40mA (V_{OH}=3.5V@VDD=5V).

4.8 Communication Module

4.8.1 SPI Module

The SPI is a fully configurable SPI master/slave device that allows the user to configure the polarity and phase of the serial clock signal. SPI allows the MCU to communicate with serial peripherals, and it is also capable of inter processor-to-processor communication in multi-host systems. SPI has the following features:

- Full-duplex synchronous serial data transfer.
- Supports master/slave mode.
- Support for multi-host systems.
- System error detection.
- Supports speeds up to 1/4 of the system clock (F_{SYS}≤24MHz).
- The bit rate produces 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512 of the system clock.
- Four transmission formats are supported.
- Send/receive completion can produce an interrupt.

4.8.2 I²C Module

The two-wire bidirectional serial bus controller I2C provides a simple and efficient connection for data exchange between the microprocessor and the I2C bus. The I2C module has the following features:

- Support 4 working modes: master transmission, master reception, slave transmission, slave reception.
- Supports 2 transfer speed modes:
  Standard (up to 100Kb/s);
  Fast (up to 400Kb/s).
- Perform arbitration and clock synchronization.
- Support for multi-host systems.
- The host mode supports7-bit addressing mode and 10-bit addressing mode on the I2C-bus (software supported).
- Slave mode supports7-bit addressing mode on the I2C-bus.
- Allows operation over a wide clock frequency range (built-in 8-bit timer).
- Receive/send completion can produce an interrupt.

4.8.3 UARTn Module

The UARTn module contains UART0/UART1, 2 serial ports with exactly the same function. UARTn has the following features:

- Full-duplex serial port.
- Synchronous mode is supported.
- Supports 8-bit asynchronous transceiver mode with variable baud rate.
- Supports a 9-bit asynchronous transceiver mode with variable baud rate
- Baud rates can be generated by timer1/Timer4/Timer2/BRT modules.
- Send/receive completion can produce an interrupt.

4.9 Analog Module

4.9.1 Analog-to-digital Converter (ADC)

The ADC module is a 12-bit successive approximation analog-to-digital converter. The port analog input signal is connected to the input of the analog-to-digital converter after passing through a multiplexer, which generates a 12-bit binary result based on the input analog signal and saves the result in the ADC result register. ADCs have the following characteristics:

- Up to 30 external channels.
- The conversion clock of the ADC is available in eight clock frequencies.
- The ADC reference voltage can be selected from VDD/1.2V/2.0V/2.4V/3.0V.
- A full 12-bit conversion requires 18.5 ADC conversion cycles.
- Supports external port edges, PWM trigger ADC conversion.
- Supports ADC conversion result comparison output.
- Supports interrupt generation when an ADC conversion is complete.

4.9.2 Touch Module (TOUCH)

The touch module is an integrated circuit designed to realize the human touch interface, which can replace the mechanical light touch button to achieve waterproof and dustproof, sealed isolation, strong and beautiful operation interface.

Technical parameters:

- Up to 26 touch buttons are available.
- No external touch capacitors are required.
- The effective touch response time is less than 100ms.

4.10 FLASH Memory

The FLASH memory contains program memory (APROM/BOOT) and non-volatile data memory (Data FLASH) that can be accessed by the associated special function register (SFR) to achieve IAP functionality. Flash memory supports the following operations:

- Byte read operation.
- Byte write operations.
- Page erase operation.
- FLASH space CRC check operation.

4.11 Unique ID (UID)

Each chip has a 96-bit unique identification number, known as Unique identification. The UID is already set at the factory and cannot be modified by the user.

5. User Configuration

The System Configuration Register (CONFIG) is a FLASH option for the initial conditions of the MCU and cannot be accessed or operated by the program. The System Configuration Register allows you to set the following:

- The way watchdogs work.
- FLASH program area partition protection, code encryption, FLASH data area encryption status.
- Low voltage reset voltage.
- Debug mode disable or enable.
- Oscillation mode, prescale selection.
- Internal high-speed oscillator frequency division selection.
- Sleep wake-up wait time.
- APROM/BOOT space.

6. Electrical Parameters

6.1 Absolute Maximum Rating

symbol	parameter	minimum	maximum	unit
T_{ST}	Storage temperature	-55	150	℃
T_A	Operating temperature	-40	105	℃
VDD-VSS	Supply voltage	-0.3	5.8	V
IN_{AND}	Input voltage	VSS-0.3	VDD+0.3	V
I_{DD}	VDD maximum input current	-	120	mA
I_{SS}	VSS maximum output current	-	200	mA
THE_{IOs}	Maximum sink current for a single IO	-	50	mA
	Maximum Sink Current for a Single IO (LED COM)	-	150	mA
	Maximum current for a single IO	-	40	mA
	Single IO Maximum Current Pull (LED SEG)	-	40	mA
	Maximum sink current for all IO	-	200	mA
	Maximum pull current for all IO	-	120	mA

Note: If the operating conditions of the device exceed the range of "**absolute maximum rating**", it will cause permanent damage to the device. The function can be guaranteed only when the device works within the scope specified in the manual. The chip is at the absolute maximum rated value, which may affect the reliability of the device.

6.2 DC Electrical Characteristics

VDD-VSS=2.1～5.5V，T_A=25℃

symbol	parameter	Test conditions	minimum	Typical	maximum	unit
VDD	Operating voltage	F_{SYS}=48MHz，F_{CPU}=F_{SYS}/2 F_{SYS}=8MHz~24MHz，F_{CPU}=F_{SYS}	2.1	-	5.5	V
I_{DD}	Normal mode	VDD=5V, F_{SYS}=48MHz, all peripherals off F_{CPU}=F_{SYS}/2	-	8	-	mA
		VDD=3V, F_{SYS}=48MHz, all peripherals off F_{CPU}=F_{SYS}/2	-	8	-	mA
		VDD=5V, F_{SYS}=24MHz, all peripherals are off F_{CPU}=F_{SYS}	-	5	-	mA
		VDD=3V, F_{SYS}=24MHz, all peripherals are off F_{CPU}=F_{SYS}	-	5	-	mA
		VDD=5V, F_{SYS}=16MHz, all peripherals are off F_{CPU}=F_{SYS}	-	4	-	mA
		VDD=3V, F_{SYS}=16MHz, all peripherals are off F_{CPU}=F_{SYS}	-	4	-	mA
		VDD=5V, F_{SYS}=8MHz, all peripherals off F_{CPU}=F_{SYS}	-	3	-	mA
		VDD=3V, F_{SYS}=8MHz, all peripherals are off F_{CPU}=F_{SYS}	-	3	-	mA
		VDD=5V, F_{SYS}=32.7678KHz, all peripherals off F_{CPU}=F_{SYS}	-	0.35	-	mA
		VDD=3V, F_{SYS}=32.7678KHz, all peripherals are off F_{CPU}=F_{SYS}	-	0.31	-	mA
	IDLE mode (CPU stopped).	VDD=5V, F_{SYS}=48MHz, all peripherals off	-	7	-	mA
		VDD=3V, F_{SYS}=48MHz, all peripherals off	-	7	-	mA
		VDD=5V, F_{SYS}=24MHz, all peripherals are off	-	4	-	mA
		VDD=3V, F_{SYS}=24MHz, all peripherals are off	-	4	-	mA
		VDD=5V, F_{SYS}=16MHz, all peripherals are off	-	3.5	-	mA
		VDD=3V, F_{SYS}=16MHz, all peripherals are off	-	3.5	-	mA
		VDD=5V, F_{SYS}=8MHz, all peripherals off	-	2.5	-	mA
		VDD=3V, F_{SYS}=8MHz, all peripherals are off	-	2.5	-	mA
		VDD=5V, F_{SYS}=32.768KHz, all peripherals are off	-	0.35	-	mA
		VDD=3V, F_{SYS}=32.768KHz, all peripherals are off	-	0.31	-	mA
I_{SLEEP1}	Sleep current	All peripherals are off, 32.768KHz timer enabled, LVR shutdown	-	20	-	uA
I_{SLEEP2}	Sleep current	All peripherals are off, LSI, WUT timer enabled, LVR off	-	7	-	uA
I_{SLEEP3}	Sleep current	All peripherals are off, LVR is off	-	6	-	uA
I_{LI}	Input leakage	-	-	-	0.1	uA
V_{IL}	input low voltage	-	VSS	-	0.3VDD	V
V_{IH}	Enter high voltage	-	0.7VDD	-	VDD	V
V_{OL}	Output low voltage	VDD=5V,I_{OL1}=18mA	-	-	0.4	V
		VDD=5V，I_{OL2}=50mA（LED COM）	-	-	0.4	V
		VDD=3V,I_{OL1}=12mA	-	-	0.4	V
		VDD=3V，I_{OL2}=22mA（LED COM）	-	-	0.4	V
V_{OH}	Output high	VDD=5V,I_{OH1}=35mA	3.5	-	-	V

	voltage	VDD=5V,I_{OH2}=35mA （LED SEG Max）	3.5	-	-	V
		VDD=5V,I_{OH3}=2.6mA (LED HIMSELF Min)	3.5	-	-	V
		VDD=3V,I_{OH1}=13.5mA	2.1	-	-	V
		VDD=3V,I_{OH2}=13.5mA （LED SEG Max）	2.1	-	-	V
		VDD=3V,I_{OH3}=1mA(LED MIN)	2.1	-	-	V
R_{PH}	Pull-up resistor	-	-	32	-	KΩ
R_{PL}	Pull-down resistor	-	-	32	-	KΩ

6.3 AC Electrical Parameters

6.3.1 Power-up and Power-down Operation

T_A= 25°C, excluding 32.768K crystal resonant time

symbol	parameter	Test conditions	minimum	Typical	maximum	unit
T_{RESET}	Reset time	VDD=5V	-	16	-	ms
TVDDR	VDD rise rate	VDD=5V	20	-	-	us/V
TVDDF	VDD fall rate	VDD=5V	20	-	-	us/V

6.3.2 External Oscillator

symbol	parameter	Test conditions	minimum	Typical	maximum	unit
V_{HSE}	Operating voltage	F=8/16MHz, C_{XT}=0-47pF	2.1	-	5.5	V
V_{LSE}	Operating voltage	F=32.768KHz, C_{XT}=10-22pF	2.1	-	5.5	V

6.3.3 Internal Oscillator

VDD=2.1V-5.5V

symbol	parameter	Test conditions	Frequency error	minimum	Typical	maximum	unit
F_{HSI}	Internal high speed 48MHz	T_A=25℃	±1%	-	48	-	MHz
		T_A=-20℃ to 85℃	±2%	-	48	-	MHz
		T_A=-40℃ to 105℃	±3%	-	48	-	MHz
F_{LSI}	Internal low speed 125KHz	T_A=25℃	±5%	-	125	-	KHz
		T_A=-40℃ to 105℃	±50%	-	125	-	KHz

6.3.4 Low-voltage Reset Electrical Parameters

symbol	parameter	minimum	Typical	maximum	unit
V_{LVR1}	Low pressure detection threshold 1.8V	1.65	1.8	1.95	V
V_{LVR2}	Low pressure detection threshold 2.0V	1.85	2.0	2.15	V
V_{LVR3}	Low pressure detection threshold 2.5V	2.35	2.5	2.65	V
V_{LVR4}	Low pressure detection threshold 3.5V	3.35	3.5	3.65	V

6.3.5 LVD Electrical Parameters

symbol	parameter	minimum	Typical	maximum	unit
V_{LVD1}	Low pressure detection threshold 2.0V	1.85	2.0	2.15	V
V_{LVD2}	Low pressure detection threshold 2.2V	2.05	2.2	2.35	V
V_{LVD3}	Low pressure detection threshold 2.4V	2.25	2.4	2.55	V
V_{LVD4}	Low pressure detection threshold 2.7V	2.55	2.7	2.85	V
V_{LVD5}	Low pressure detection threshold 3.0V	2.85	3.0	3.15	V
V_{LVD6}	Low pressure detection threshold 3.7V	3.55	3.7	3.85	V
V_{LVD7}	Low pressure detection threshold 4.0V	3.85	4.0	4.15	V
V_{LVD8}	Low pressure detection threshold 4.3V	4.15	4.3	4.45	V

6.4 FLASH Electrical Parameters

symbol	parameter	Test conditions	minimum	Typical	maximum	unit
V_F	FLASH operating voltage	-	2.1	-	5.5	V
T_F	FLASH operating temperature	-	-40	27	105	℃
$N_{ENDURANCE}$	The number of erases and writes	Program FLASH	20,000	-	-	Cycle
		Data FLASH	100,000	-	-	Cycle
T_{RET}	Data retention time	25℃	100	-	-	year
T_{ERASE}	Sector erase time	-	-	1.5	-	ms
T_{PROG}	Programming time	-	-	7	-	us
I_{DD1}	Read current	-	-	-	2.5	mA
I_{DD2}	Programming the current	-	-	-	3.6	mA
I_{DD3}	Erase the current	-	-	-	2	mA

6.5 Simulation Characteristics

6.5.1 BANDGAP Electrical Characteristics

T_A=25℃

symbol	parameter	Test conditions	minimum	Typical	maximum	unit
V_{BG}	Internal reference 1.2V	VDD=2.1~5.5V、T_A=25℃	1.188	1.2	1.212	V
		VDD=2.1~5.5V、T_A=-20℃ to 85℃	1.182	1.2	1.218	V
		VDD=2.1~5.5V、T_A=-40℃ to 105℃	1.176	1.2	1.224	V

6.5.2 ADC Electrical Characteristics

T_A=25℃

symbol	parameter		minimum	Typical	maximum	unit
V_{AVDD}	ADC operating voltage		2.5	-	5.5	V
V_{REF1}	Reference voltage 1		-	IN_{AVDD}	-	V
V_{REF2}	Reference voltage 2 (non-V_{BG}).		1.185	1.2	1.215	V
V_{REF3}	Reference voltage 3		1.985	2.0	2.015	V
V_{REF4}	Reference voltage 4		2.385	2.4	2.415	V
V_{REF5}	Reference voltage 5		2.985	3.0	3.015	V
V_{ADI}	Input voltage		0	-	V_{REF}	V
N_R	resolution		12			Bit
DNL	Differential nonlinearity error (V_{REF}=V_{AVDD}=5V, T_{ADCK}=0.5us).		±2			LSB
INL	Integral nonlinearity error (V_{REF} =V_{AVDD}=5V, T_{ADCK}=0.5us).		±4			LSB
T_{ADCK}	ADC clock cycle	V_{REF}=VDD=5V	0.5	-	-	us
		V_{REF}=V_{REF2}	32	-	-	us
		V_{REF} =V_{REF3}/ V_{REF4}/V_{REF5}	2	-	-	us
T_{ADC}	ADC conversion time		-	18.5	-	T_{ADCK}
F_S	sample rate(V_{REF}=V_{AVDD}=5V)		100			Ksps

Note: When V_{REF} = V_{REF2}, the precision is 8-bit.

6.6 EMC Features

6.6.1 EFT Electrical characteristics

symbol	parameter	Test conditions	grade
V_{EFTB}	Fast transient voltage burst limits to beapplied through 0.1uF(capacitance) on VDDand VSSpins to induce a functional disturbance	T_A = + 25℃, F_{SYS}=48MHz, conforms to IEC 61000-4-4	4B

Note: The immunity performance of electrical fast transient pulse swarm (EFT) is closely related to the system design (including power supply structure, circuit design, layout and wiring, chip configuration, program structure, etc.). The EFT parameters in the table above are measured on the CMS internal test platform and are not suitable for all application environments, and the test data is for reference only. All aspects of the system design may affect the EFT performance, in the application of high EFT performance requirements, the design should pay attention to avoid interference sources affecting the operation of the system, it is recommended to analyze the interference path and optimize the design to achieve the best immunity performance.

6.6.2 ESD electrical characteristics

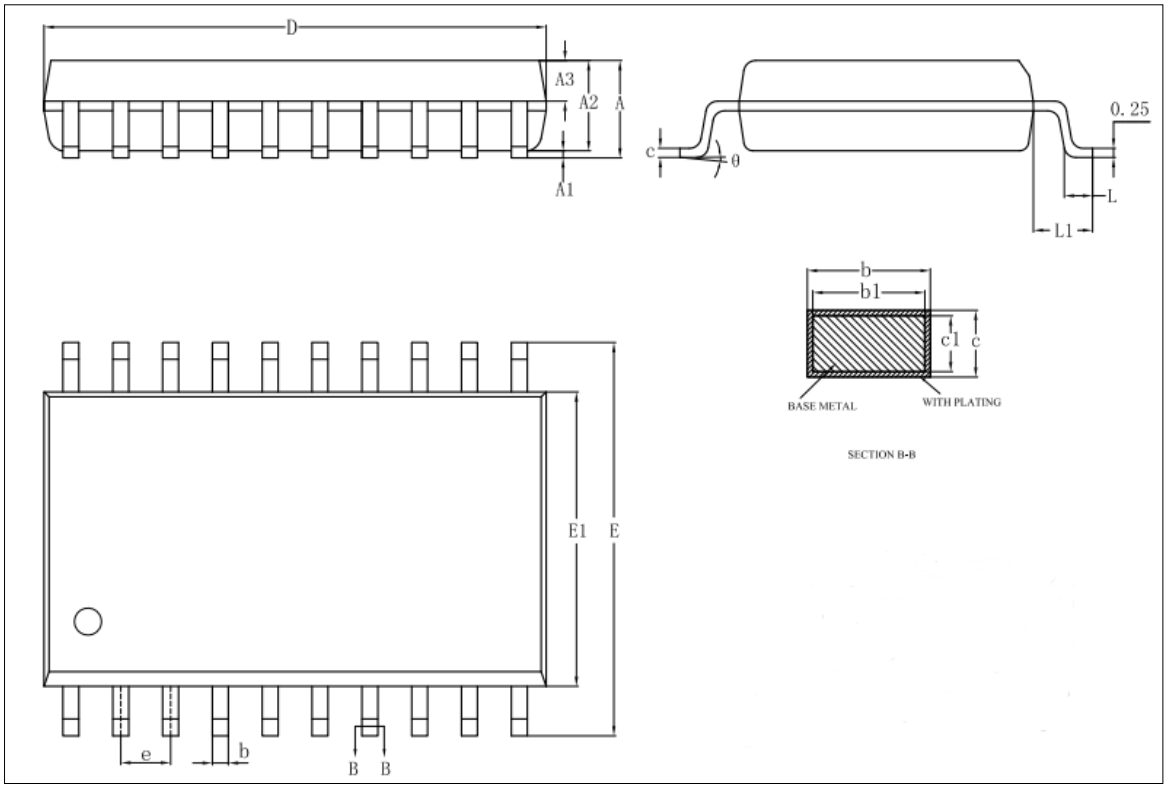
symbol	parameter	Test conditions	grade
V_{ESD}	Electrostatic discharge (Human discharge mode HBM)	T_A = + 25℃, JEDEC EIA/JESD22- A114	3B
	Electrostatic discharge (Machine discharge mode MM)	T_A = + 25℃, JEDEC EIA/JESD22- A115	C

6.6.3 Latch-Up electrical characteristics

symbol	parameter	Test conditions	The test type
LU	Static latch-up class	JEDEC STANDARD NO.78D NOVEMBER 2011	Class I (T_A = +25℃)

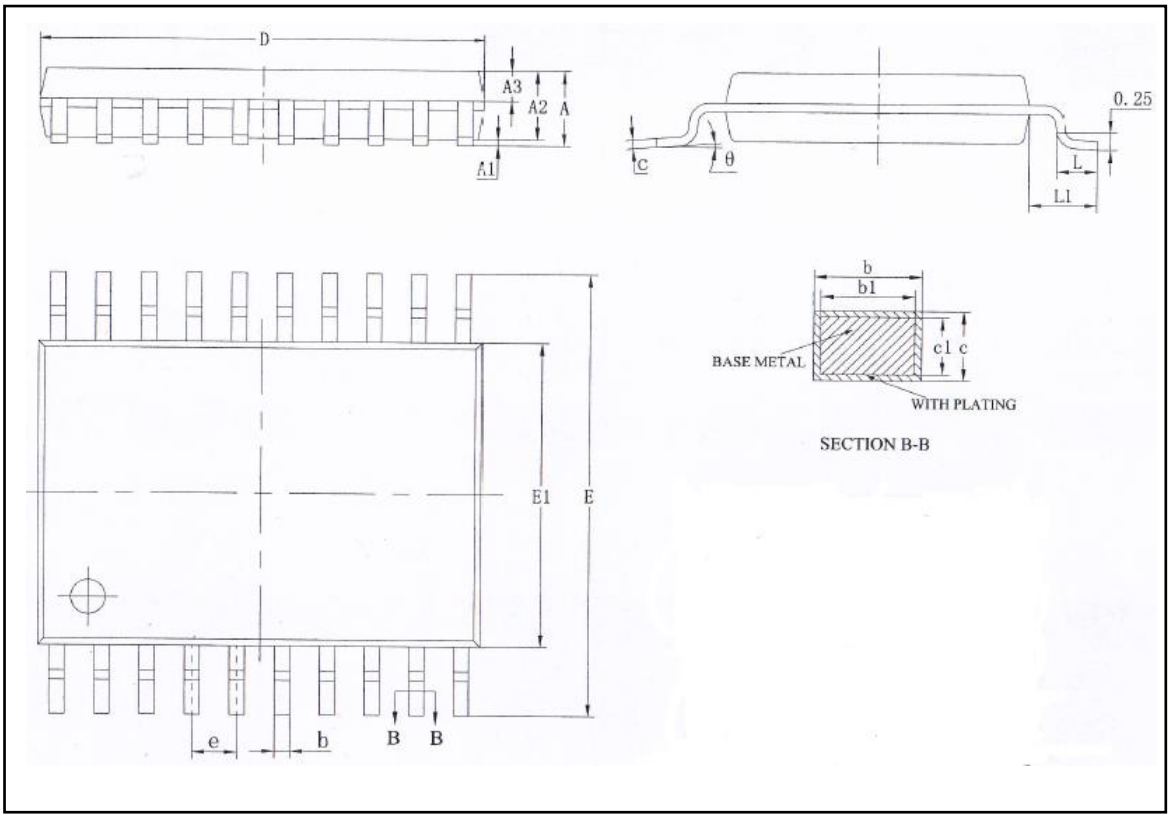
7. Packaging Information

7.1 SOP20



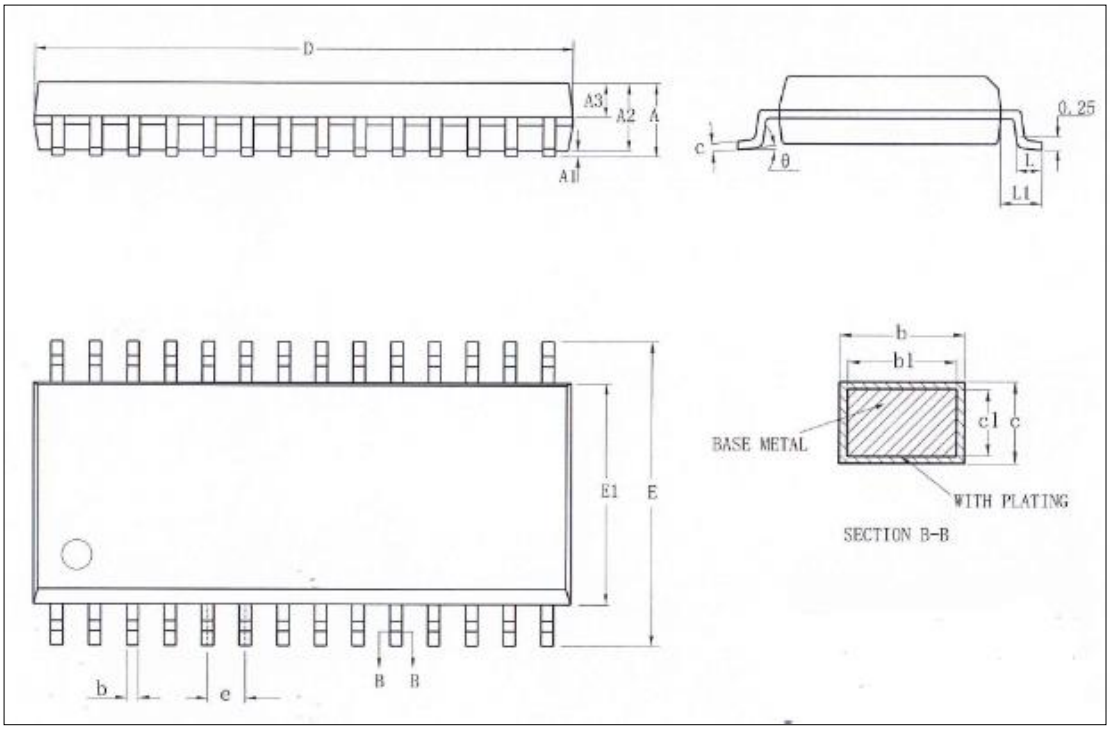
Symbol	Millimeter		
	Min	Nom	Max
A	-	-	2.65
A1	0.10	-	0.30
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.39	-	0.47
b1	0.38	0.41	0.44
c	0.25	-	0.29
c1	0.24	0.25	0.26
D	12.70	12.80	12.90
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.27BSC		
L	0.70	-	1.00
L1	1.40REF		
θ	0	-	8°

7.2 TSSOP20



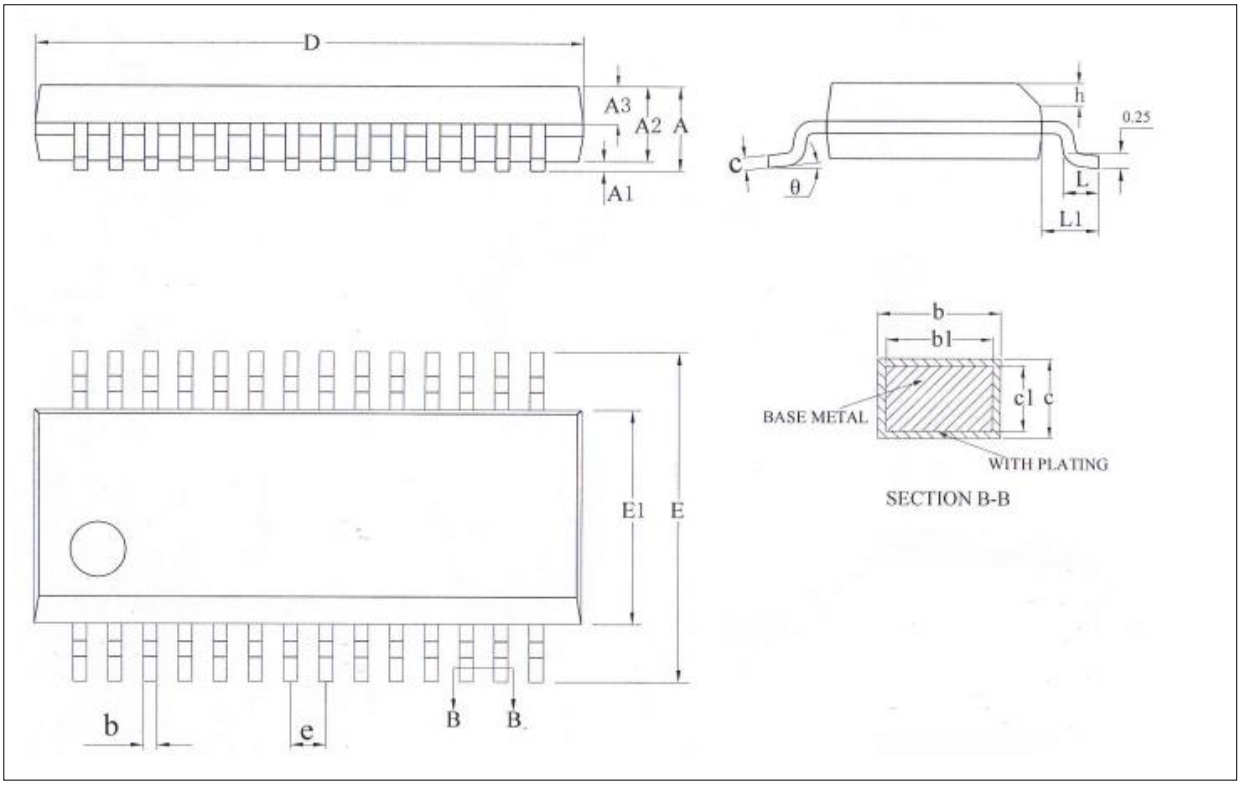
Symbol	Millimeter		
	Min	Nom	Max
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	-	0.28
b1	0.19	0.22	0.25
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	6.40	6.50	6.60
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00REF		
θ	0	-	8°

7.3 SOP28



Symbol	Millimetre		
	Min	Nom	Max
A	-	-	2.65
A1	0.10	-	0.30
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.39	-	0.47
b1	0.38	0.41	0.44
c	0.25	-	0.29
c1	0.24	0.25	0.26
D	17.90	18.00	18.10
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.27BSC		
L	0.70	-	1.00
L1	1.40REF		
θ	0	-	8°

7.4 SSOP28



Symbol	Millimeter		
	Min	Nom	Max
A	-	-	1.75
A1	0.05	-	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.23	-	0.31
b1	0.22	0.25	0.28
c	0.20	-	0.24
c1	0.19	0.20	0.21
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	0.635BSC		
h	0.25	-	0.50
L	0.50	-	0.80
L1	1.05REF		
θ	0	-	8°

8. Version History

Revision	Date	Modify content
V1.00	Sep 2020	Initial release
V1.0.1	Apr 2023	1) Added CMS80F7316-TSSOP20 and CMS80F7318-SSOP28 models and related information 2) Update 6.6 EMC Features 3) Update 7.1 packaging Information
V1.0.2	Aug 2023	1) 6.1 Absolute Maximum Rating: add limit parameter notes 2) 6.3.1 Power-up and Power-down Operation: adjust parameters 3) 6.3.3 Internal Oscillator: adjust parameters 4) 6.5.1 BANDGAP Electrical Characteristics: detailed parameters 5) 6.5.2 ADC Electrical Characteristics: ADC clock cycle is described according to different reference voltages 6) Update 7.4 packaging Information